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EXAMINER
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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Paper No. 7

Application Number: 10/017, 031

Filing Date: October 30, 2001

Appellant(s): David A. Kiss

Timothy N. Trop

Trop, Prumer and Hu, P.C.

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 24, 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

The rejection of claims 1-24 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,276,834	Mauritz et al	1-1994
6,376,904	Haba et al	4-2002
6,236,109	Hsuan et al	5-2001
6,225,688	Kim et al	5-2001

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 18 are rejected under 35 U.S.C. 102 (b)). This rejection is set forth in prior Office Action, Paper No. 4.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Mauritz et al..

Mauritz teaches in figures 1 and 2 integrated circuit packages having plurality of chips including a processor 12, cross point memory in a spare chip 22 and at least one volatile memory chips 19 (see col. 1, DRAM). The claims fail to characterize the term "packaging". As semiconductor memory chips and DRAMS are typically packaged chips the invention of Mauritz is deemed to be inherently packaged.

Claims 1-24 are rejected under 35 U.S.C. 1-3 (a). This rejection is set forth in prior Office Action, Paper No. 4.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haba et al in view of Mauritz et al, Hsuan et al (6,236,109) and Kim et al.

Haba et al shows a package integrated circuit comprising processor and a plurality of memory die (see col.1, lines 10-12). As the claims fail to provided specific structure characteristic of "package" Haba is utilized in this rejection to show specific " package" features (i.e bus structure, encapsulation425, substrate 420 , chips 440, ball grid array 455, etc.) containing memory chip structure. It has long been the convention in this technology to provide several types of memory devices and processors in a single package to reduce processing costs, package volume, improve signal transmission. The focus of the teachings of Haba et al is a package arrangement that may employ the conventional chips recited in the claims of the instant invention.

Haba et al also clearly teaches the convention of packaging the types of devices including first die second die stacked memory structures recited in for example claims 5, 15, 18 and 23 of the instant invention in a single package but fails to teach a folded stack and the specific types of memory claimed. It is also however deemed that Haba et al suggests use of conventional memory devices that may be utilized in this art which would include those recited in the claims but however fail to characterize these devices specifically as recited.

Mauritz teaches in figures 1 and 2 integrated circuit packages having plurality of chips including a processor 12, cross point memory in a spare chip 22 and volatile memory 19 and (claim 7) and non-volatile memory chip 16. It would have been obvious to one having ordinary skill in this are that these specific types of devices may be employed in the chip arrangement of Haba et al because it has long been the convention in this technology to provide several types of memory devices and processors in a single package to reduce processing costs, package volume, improve signal transmission as Hsuan also teaches in col.1, line 35-41. Haba et al in col. 1, lines 10-12, also suggests use of packages having a plurality of memory and

processors similar to the structure recited in the claims whereby said memory may be conventional memory such as volatile memory, cross point and phase change.

Folded stacked structures would be further obvious in view of the teachings of Kim et al who shows package chips in folded arrangements. It would have been obvious to one having ordinary skill in this art that that the stacked package of Haba et al could be packaged in a folded arrangement because the folded arrangement would allow for an alternative connection to each substrate similar to the connection shown in figure 7D. of Haba et al.

The ball grid array recited in the claims is also taught by Haba on the bottom surface of substrate 420 and Haba et al , Mauritz et al and Kim et al all show bus structures that are typical of package structure.

The invention of Haba et al is deemed to inherently utilize the steps of providing, coupling and packaging.

(11) Response to Argument

Applicant argues that Mauritz teaches away from putting all components in one package and relays that the package of the instant invention is a single package solution. The claims of the instant invention however fail to specifically describe what characterizes a "package" and further fails to slepcifially define or recite a "single package" and chips or compoents formed in a " single package". The claims recite only a "packaged integrated cirtuit conmprising". A "package" or " packaged" device may be formed in many different structural formats including several chips packaged within a package. Clearly Mauritz, Haba et al and Kim all teach the extent of which chips may be conventionally packaged. With more specific details recited in the claims one can not know the details of the "this" package the applicant argues. Applicant argues that Mauritz et al fails to show a package but Mauritz et al details in col. 1, lines 38 that his invention

is relative to memory arrays suchs as DRAMs which are chips that may be conventionally package in a single package.

Further contrary to the applicant assertions the teaching of Mauritz of a DRAM clearly teaches use of volatile memory as taught on page 1 of the disclosure in prior art teachings of the instant invention.

Multiple memory chip structures are commonly packaged in a single package and therefore forming the integrated chip structure are known. Applicant admits that use of the various memories recited in his claims such as volatile and cross point are not ~~know~~ new and memories are generally associated with CPUs or processors which are also not new.

Without specific structural features that fully characterize what the claims mean by " package", it can not be determined what is meant by "package" when a "package" can have variety of definitions and structural characteristics.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Sheila V. Clark

July 14, 2003

SHEILA V. CLARK
PRIMARY EXAMINER

Appeal Conferees: Mr. Eddie Lee

Mr. Olik Chaudhuri